Remarks

The Office Action mailed April 10, 2001 has been received and reviewed. Claims 27, 30, 32, 34, and 36 have been amended. Therefore, claims 27-38 are pending. Claim 30 was amended to correct for improper dependency.

The Claim Objection

The Examiner objected to claim 36 indicating that a typographical error exists on line 4 thereof. Applicant does not believe that an error exists, but would be more than willing to discuss this claim with the Examiner. As such, no amendment to correct a typographical error was made. Applicant respectfully requests reconsideration and withdrawal of the objection.

The 35 U.S.C. §102 Rejections

The Examiner rejected claims 27-35 under 35 U.S.C. §102(b) as being anticipated by Matsubara et al. (U.S. Patent No. 5,122,923). Specifically, the Examiner alleges that Matsubara et al. discloses a thin-film capacitor comprising a lower electrode, a dielectric layer, and an upper electrode. The lower electrode is alleged to be made from $RuSi_2$ and may consist of layers of ruthenium, ruthenium oxide, ruthenium oxide, ruthenium silicide and stacked structures.

Applicants respectfully traverse the Examiner's rejection. However, the claims have been amended to move the case forward to allowance. In particular, the claims have been amended to indicate that the diffusion barrier layer is formed using chemical vapor deposition.

For a claim to be anticipated under 35 U.S.C. § 102(b), each and every element of the claim must be found in a single prior art reference. *See* M.P.E.P. § 2131.

Matsubara et al. describes a sputtered $RuSi_2$ layer and not a diffusion barrier layer formed using chemical vapor deposition. A diffusion barrier layer formed using chemical vapor deposition as described according to the present invention is different than the layer sputtered according to Matsubara et al.

As such, for at least this reason, claims 27-35 are not anticipated by Matsubara et al. Applicant respectfully requests reconsideration and withdrawal of the rejection.

The Examiner also rejected claims 36-38 under 35 U.S.C. §102(b) as being anticipated by Chin et al. (U.S. Patent No. 5,491,365). Specifically, the Examiner alleges that Chin discloses an integrated circuit device comprising a substrate, contact, and contact diffusion barrier.

Applicants respectfully traverse the Examiner's rejection. However, the claims have been amended to move the case forward to allowance. In particular, the claims have been amended to indicate that the diffusion barrier layer is formed using chemical vapor deposition.

For a claim to be anticipated under 35 U.S.C. § 102(b), each and every element of the claim must be found in a single prior art reference. *See* M.P.E.P. § 2131.

Chin describes a barrier layer formed by implanting a component of the barrier into a resistivity material to establish a material that comprises the barrier and does not describe a diffusion barrier layer formed using chemical vapor deposition. A diffusion barrier layer formed using chemical vapor deposition as described according to the present invention is different than the layer formed according to Chin.

As such, for at least this reason, claims 36-38 are not anticipated by Chin. Applicant respectfully requests reconsideration and withdrawal of the rejection.

The 35 U.S.C. §103 Rejection

The Examiner rejected claims 27-35 under 35 U.S.C. §103(a) as being unpatentable over Larson (U.S. Patent No. 5,065,102) in view of Chin et al. Specifically, the Examiner alleges that Larson discloses a capacitor comprising a bottom electrode, a dielectric, and a top electrode. The bottom electrode is alleged to comprise a diffusion barrier and layers. The Examiner recognizes that Larson does not disclose a diffusion barrier layer of $RuSi_2$. However, the Examiner indicates that Chin states that $RuSi_2$ is a preferable material for a diffusion barrier and that it would have

been obvious to one of skill in the art to use such a material since it establishes good contact to an underlying semiconductor material as stated in Chin.

Applicants respectfully traverse the Examiner's rejection. However, the claims have been amended to move the case forward to allowance. In particular, the claims have been amended to indicate that the diffusion barrier layer is formed using chemical vapor deposition.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143.

The cited references do not teach or suggest all the claim limitations of the amended claims. For example, the cited references do not describe a diffusion barrier layer formed of $RuSi_x$ using chemical vapor deposition. Rather, Larson (as acknowledged by the Examiner) does not describe a $RuSi_x$ diffusion barrier layer at all, and further, Chin describes a barrier layer formed by implanting a component of the barrier into a resistivity material to establish a material that comprises the barrier and not a diffusion barrier layer formed using chemical vapor deposition.

Further, there is no teaching or suggestion to combine such references to provide a diffusion barrier layer formed of $RuSi_x$ using chemical vapor deposition. Rather, Chin actually teaches away from use of such a method of forming a $RuSi_x$. For example, as specifically described therein, a barrier layer is formed by implanting a component of the barrier into a resistivity material to establish a material that comprises the diffusion barrier. This is specifically performed to alleviate problems of other formation methods, e.g., sputtering. To form the diffusion barrier layer of Chin using chemical vapor deposition or any other method would be destroying the function of the layer formed in Chin.

As such, the pending claims are not obvious over the combination of Chin and Larson. Applicant respectfully requests reconsideration and withdrawal of the rejection.

Summary

In view of the above amendments and remarks, reconsideration and withdrawal of the rejections are respectfully requested. It is respectfully submitted that the pending claims are in condition for allowance and notification to that effect is respectfully requested. The Examiner is invited to contact Applicants' Representatives, at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

Brian A. Vaartstra et al.,

By their Representatives,
Mueting, Raasch & Gebhardt, P.A.
P.O. Box 581415
Minneapolis, MN 55458-1415
Phone: (612) 305-1220
Facsimile: (612) 305-1228
Customer Number 26813

9 July 2001
Date

By: _____
Mark J. Gebhardt
Reg. No. 35,518
Direct Dial (612)305-1216

CERTIFICATE UNDER 37 CFR §1.10:
"Express Mail" mailing label number: EL776904172US Date of Deposit: July 9 2001
The undersigned hereby certifies that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

By: _____
Name: Cara L. Ladwig

APPENDIX A - SPECIFICATION/CLAIM AMENDMENTS INCLUDING NOTATIONS TO INDICATE CHANGES MADE
Serial No.: 09/603,132
Docket No.: 150.00650102

Amendments to the following are indicated by underlining what has been added and bracketing what has been deleted.

In the Claims

For convenience, all pending claims are shown below.

27. (Once Amended) A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a diffusion barrier layer over at least a portion of the surface, wherein the diffusion barrier layer is formed of $RuSi_x$ using chemical vapor deposition, where x is in the range of about 0.01 to about 10.

28. The structure of claim 27, wherein x is in the range of about 1 to about 3.

29. The structure of claim 28, wherein x is about 2.0.

30. (Once Amended) The structure of claim [23] 27, wherein the at least a portion of the surface is a silicon containing surface and further wherein the structure includes one or more additional conductive layers over the diffusion barrier layer formed of at least one of a metal and a conductive metal oxide.

31. The structure of claim 30, wherein the one or more conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Rh, Pd, Pt, and Ir.

32. (Once Amended) A capacitor structure comprising:

a first electrode;

a high dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first and second electrode comprises a diffusion barrier layer formed of $RuSi_x$ using chemical vapor deposition, where x is in the range of about 0.01 to about 10.

33. The structure of claim 32, wherein x is in the range of about 1 to about 3.

34. (Once Amended) The structure of claim 32, wherein the first electrode comprises a diffusion barrier layer, wherein the diffusion barrier layer of the first electrode is formed on at least a portion of a silicon containing region, and further wherein the [structure includes] first electrode comprises one or more additional conductive layers formed over the diffusion barrier layer, the one or more additional conductive layers formed of at least one of a metal and a conductive metal oxide.

35. The structure of claim 34, wherein the one or more additional conductive layers are formed from materials selected from the group of RuO_2, RhO_2, MoO_2, IrO_2, Ru, Pt, and Ir.

36. (Once Amended) A integrated circuit structure comprising:

a substrate assembly including at least one active device and a silicon containing region; and

an interconnect formed relative to the at least one active device and the silicon containing region, the interconnect including a diffusion barrier layer on at least a portion of the silicon containing region, wherein the diffusion barrier layer is formed of $RuSi_x$ using chemical vapor deposition, where x is in the range of about 0.01 to about 10.

37. The structure of claim 36, wherein x is in the range of about 1 to about 3.

38. The structure of claim 36, further comprising a conductive contact material formed relative to the diffusion barrier layer.